REMARKS

This Supplemental Amendment is being filed in response to the Notice of Non-Compliant Amendment that was received by the Office of the undersigned. In response to this Notice, Applicants have provided a clean copy of the entire replacement paragraph(s)/section(s) being amended. Accordingly, entry of the amendments is respectfully requested.

Entry of the above amendment to the specification is respectfully requested. If there are any questions regarding this amendment, or the application in general, a telephone call to the undersigned would be appreciated since this expedite the prosecution of the application for all concerned.

Respectfully submitted,

Date: October 18, 2002

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EXPRESS MAIL CERTIFICATE

Date 10/18/02 Label No. EV 004809411US

I hereby certify that, on the date indicated above, this paper or fee was deposited with the U.S. Postal Service & that it was addressed for delivery to the Assistant Commissioner for Patents, Washington, DC 20231 by "Express Mail Post Office to Addressee" service.

L. DiMatteo A. DiMatteo
Name (Print) Signature

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Docket No: 3598/0G116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Sophie WILSON	Confirmation No.	5799
Serial No.:	09/395,297	Art Unit:	2183
Filed:	September 13, 1999	Examiner:	DECKTER, Stephanie M.

For: **CONDITIONAL INSTRUCTION EXECUTION IN A COMPUTER**

October 18, 2002

Assistant Commissioner for Patents
Washington, DC 20231

MARK-UP FOR SUPPLEMENTAL AMENDMENT OF OCTOBER 18, 2002 PURSUANT TO 37 C.F.R. § 1.121

IN THE SPECIFICATION:

Page 11, bridging page 12, delete the last paragraph and insert the new last paragraph as follows:

After comparing the test code specified in the addressed Treg byte with each of the condition codes CCX0 ... CCX7 (assuming the operation is being executed on the X side of the machine), then the specified operation is carried out on the SIMD lanes where there is a match, and is not carried out on the SIMD lanes where there is no match. An example is illustrated in Figure 7. Assumed that the operation illustrated in Figure 6 and described above has been carried out and that condition codes CCX0 to CCX7 have been set as described above depending on the results of the arithmetic operation in each of the SIMD lanes b_0 ...b_7. It is assumed for this example that the condition codes are $_{b0}$ 0010, b_1 0101, b_2 0011, b_3 0010, b_4 0010 b_5 0100. This is illustrated in the condition code register in Figure 7. Let us also assume that the addressed test register byte in the TST field of the instruction holds the condition code 0011. This denotes the condition Carry Set C. SIMD [lanes b_0,b_2,b_3,b_4 satisfy] satisfies this condition. Assume that the subsequent operation to be carried out is also an ADD instruction operating on the byte packed contents of two source registers SRC1,SRC2 with the results to be loaded into a destination register DST. Because a test register byte has been specified, the addition operation is only effected on the SIMD lanes where the condition code set for that lane (CCX0 ... CCX7) satisfies the condition defined by the test code set in the addressed Treg byte. This is determined by a condition code checker 50. The output of the condition code checker 50 controls a set of switches 52, one for each SIMD lane b_0 ... b_7. These switches control whether or not the results of the addition operation recited in the instruction update the values in the corresponding lane in the destination register DST. This is shown diagrammatically in Figure 7, with a cross illustrating that the result of the addition operation does not get loaded into the destination register, and a through arrow illustrating that it does. This is denoted in the destination register

by DST denoting an original byte in the destination register (that is prior to execution of the instruction), and RES denoting a result byte which, following execution of the instruction is a result of the arithmetic operation on that lane.

Respectfully submitted,

Date: October 18, 2002

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